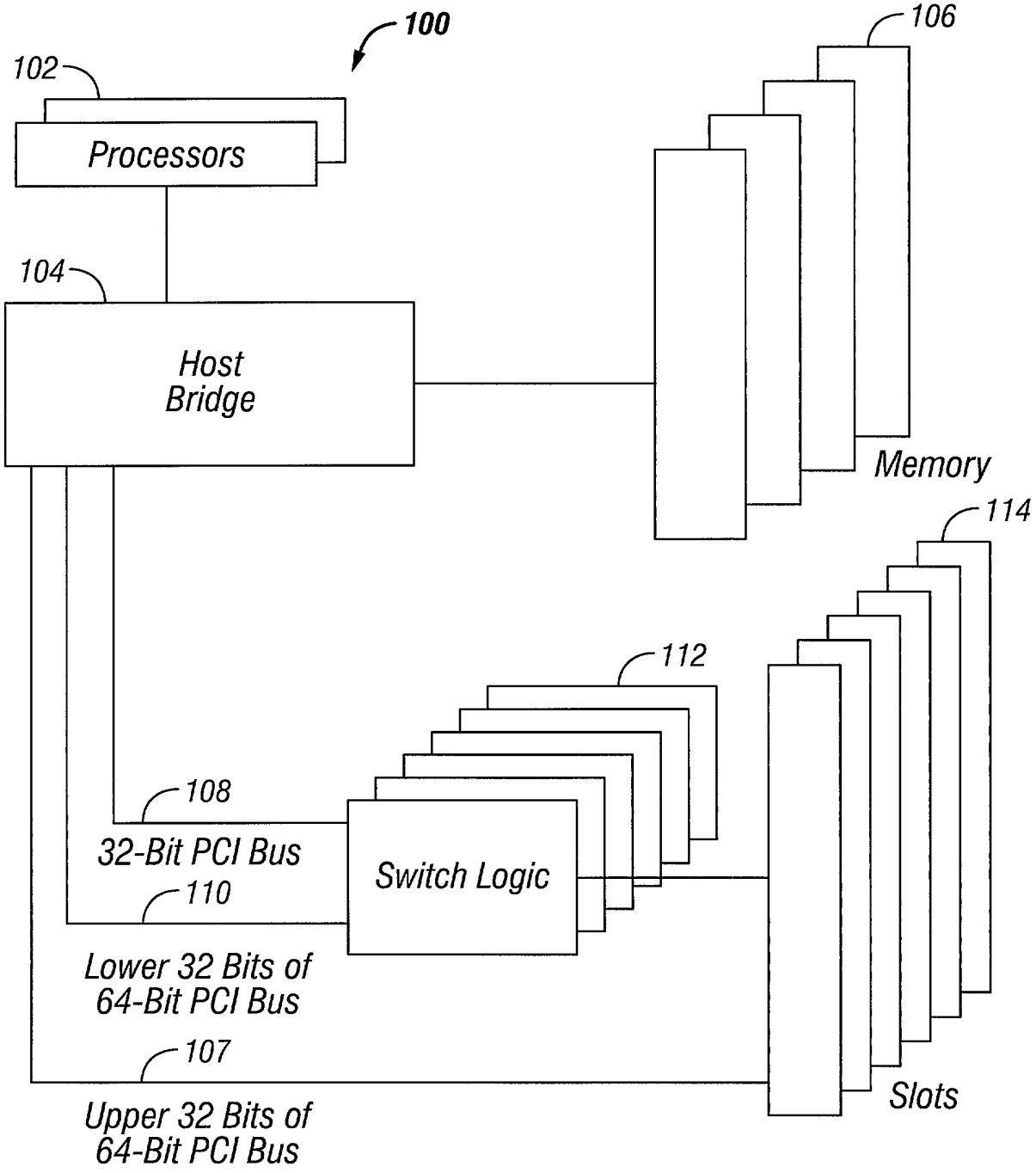
100
102
Processors
104
Host Bridge
106
Memory
114
112
108
32-Bit PCI Bus
Switch Logic
110
Lower 32 Bits of 64-Bit PCI Bus
107
Upper 32 Bits of 64-Bit PCI Bus
Slots

FIG. 1

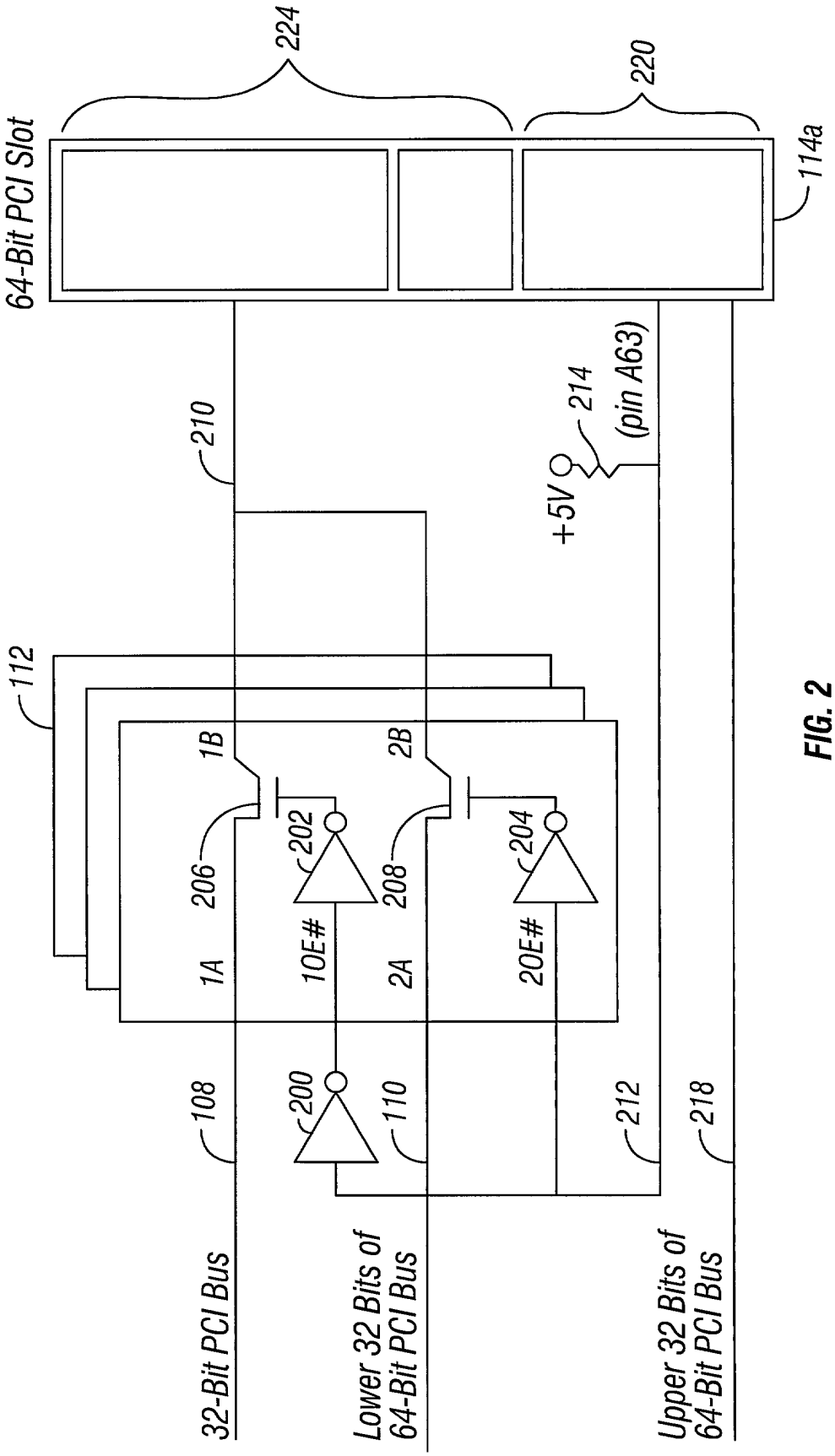
64-Bit PCI Slot
224
220
114a
210
+5V
214
(pin A63)
112
1B
2B
206
202
208
204
1A
10E#
2A
20E#
200
108
110
212
218
32-Bit PCI Bus
Lower 32 Bits of 64-Bit PCI Bus
Upper 32 Bits of 64-Bit PCI Bus

FIG. 2

300

Inputs		Inputs/Outputs	
10E#	20E#	1A, 1B	2A, 2B
L	L	1A=1B	2A=2B
L	H	1A=1B	Z
H	L	Z	2A=2B
H	H	Z	Z

FIG. 3

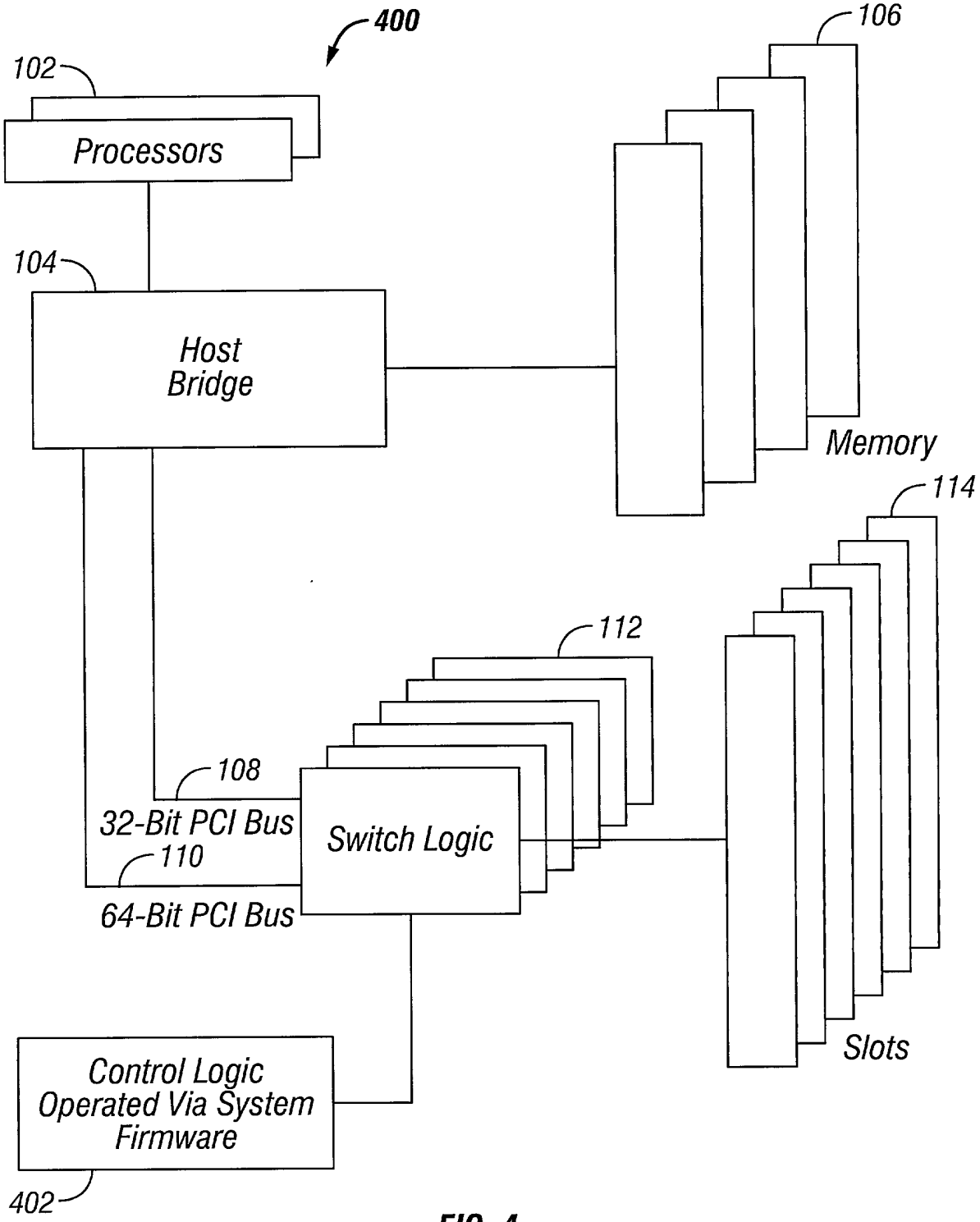
400
102
Processors
104
Host Bridge
106
Memory
114
112
108
32-Bit PCI Bus
110
64-Bit PCI Bus
Switch Logic
Slots
Control Logic Operated Via System Firmware
402

FIG. 4

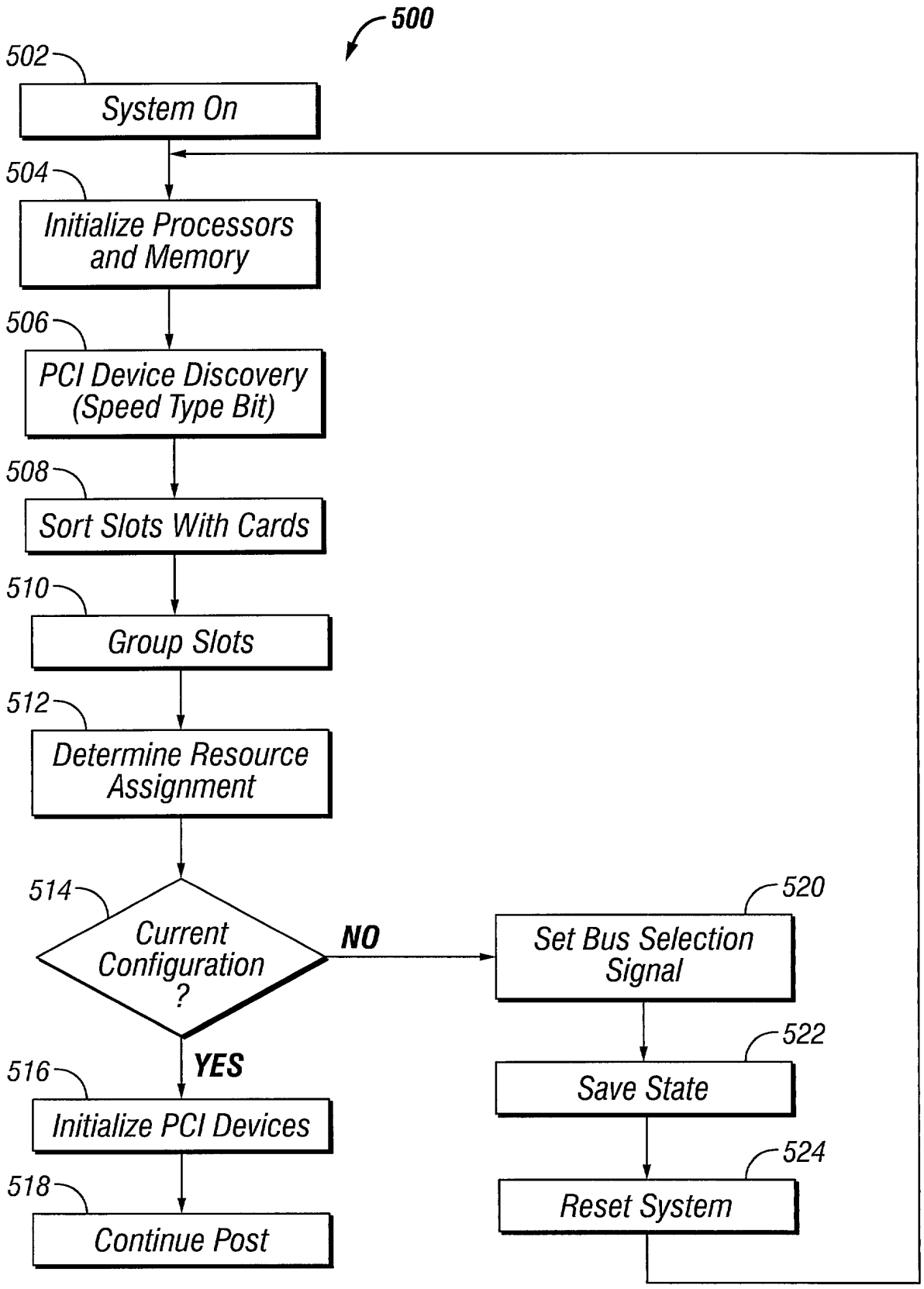
500
502
System On
504
Initialize Processors and Memory
506
PCI Device Discovery (Speed Type Bit)
508
Sort Slots With Cards
510
Group Slots
512
Determine Resource Assignment
514
Current Configuration ?
NO
YES
520
Set Bus Selection Signal
522
Save State
524
Reset System
516
Initialize PCI Devices
518
Continue Post

FIG. 5

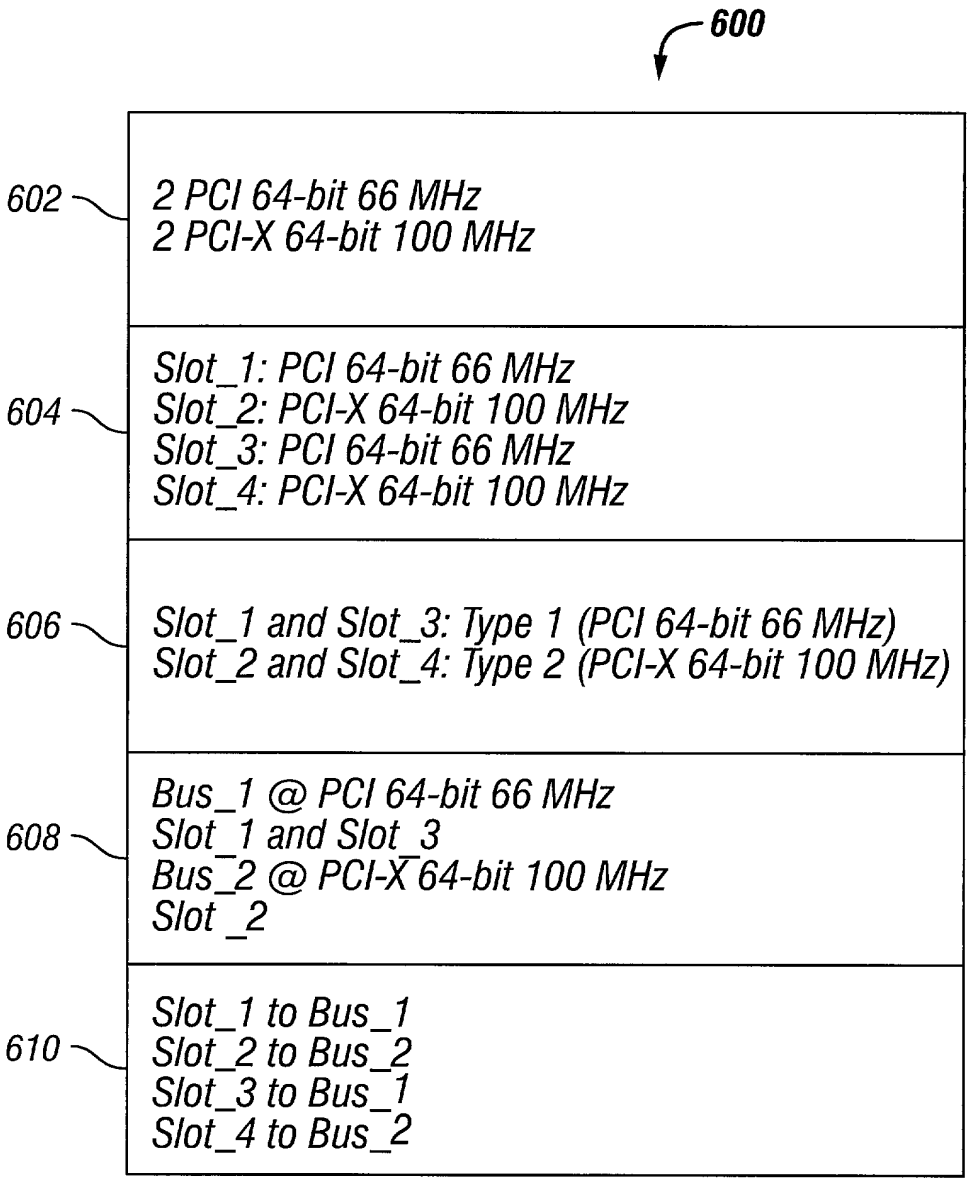
600
602
2 PCI 64-bit 66 MHz
2 PCI-X 64-bit 100 MHz
604
Slot_1: PCI 64-bit 66 MHz
Slot_2: PCI-X 64-bit 100 MHz
Slot_3: PCI 64-bit 66 MHz
Slot_4: PCI-X 64-bit 100 MHz
606
Slot_1 and Slot_3: Type 1 (PCI 64-bit 66 MHz)
Slot_2 and Slot_4: Type 2 (PCI-X 64-bit 100 MHz)
608
Bus_1 @ PCI 64-bit 66 MHz
Slot_1 and Slot_3
Bus_2 @ PCI-X 64-bit 100 MHz
Slot _2
610
Slot_1 to Bus_1
Slot_2 to Bus_2
Slot_3 to Bus_1
Slot_4 to Bus_2

FIG. 6

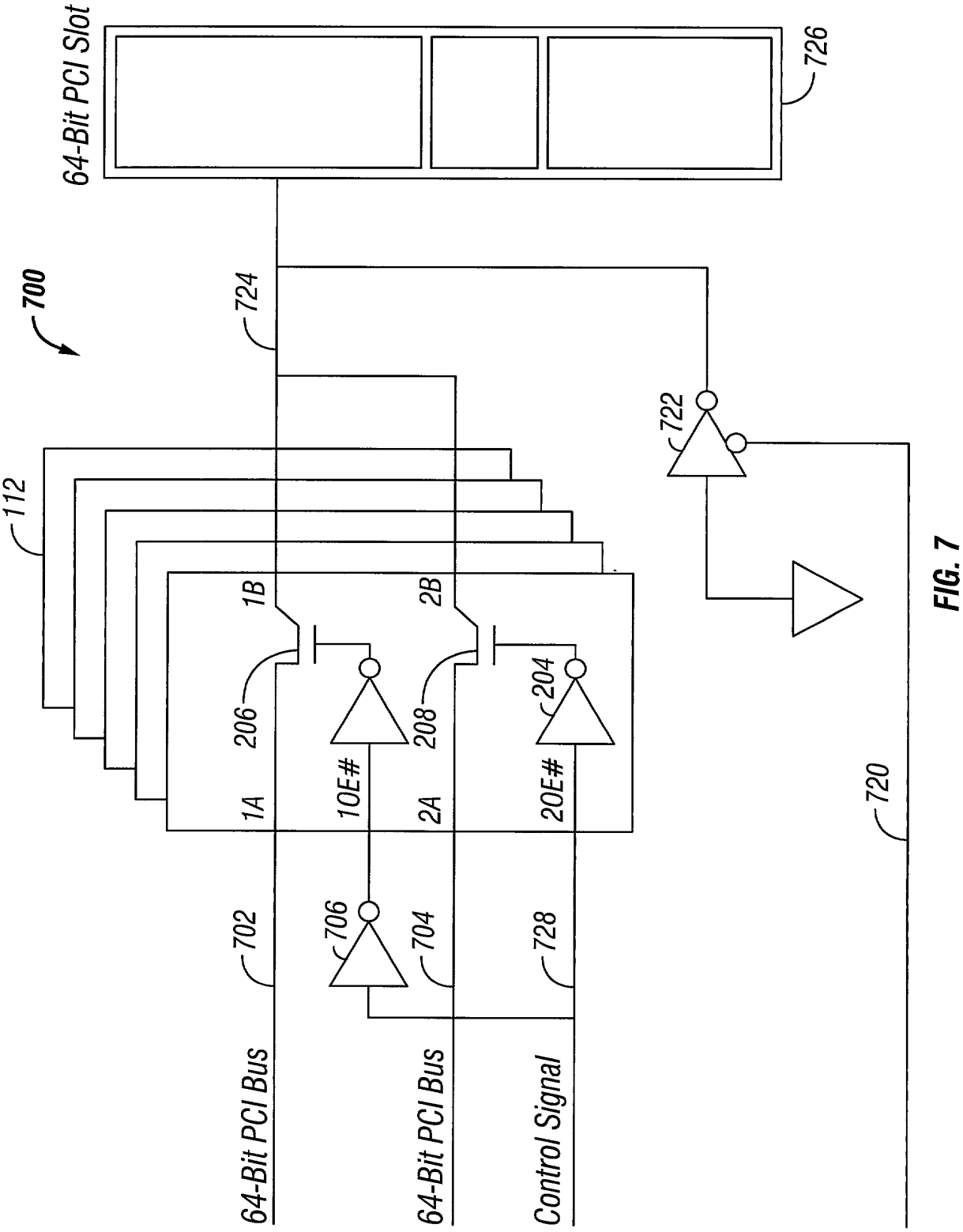
64-Bit PCI Slot
726
700
724
722
112
1B
2B
206
208
204
1A
10E#
2A
20E#
720
702
706
704
728
64-Bit PCI Bus
64-Bit PCI Bus
Control Signal

FIG. 7

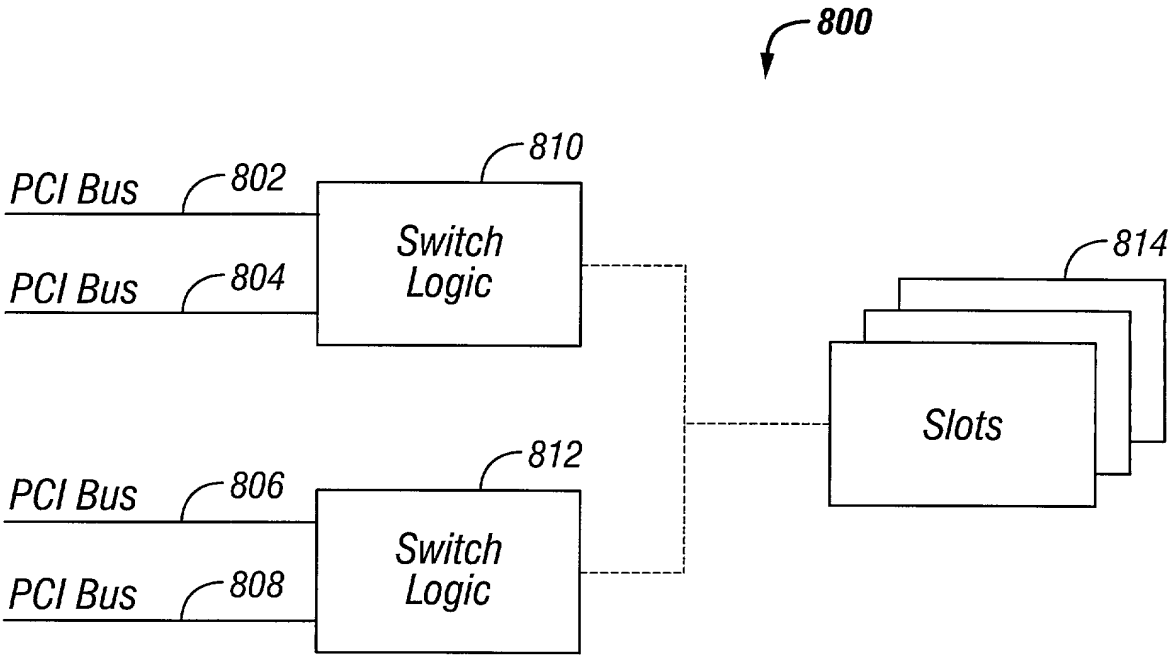
800
810
PCI Bus
802
PCI Bus
804
Switch Logic
814
Slots
812
PCI Bus
806
PCI Bus
808
Switch Logic

FIG. 8

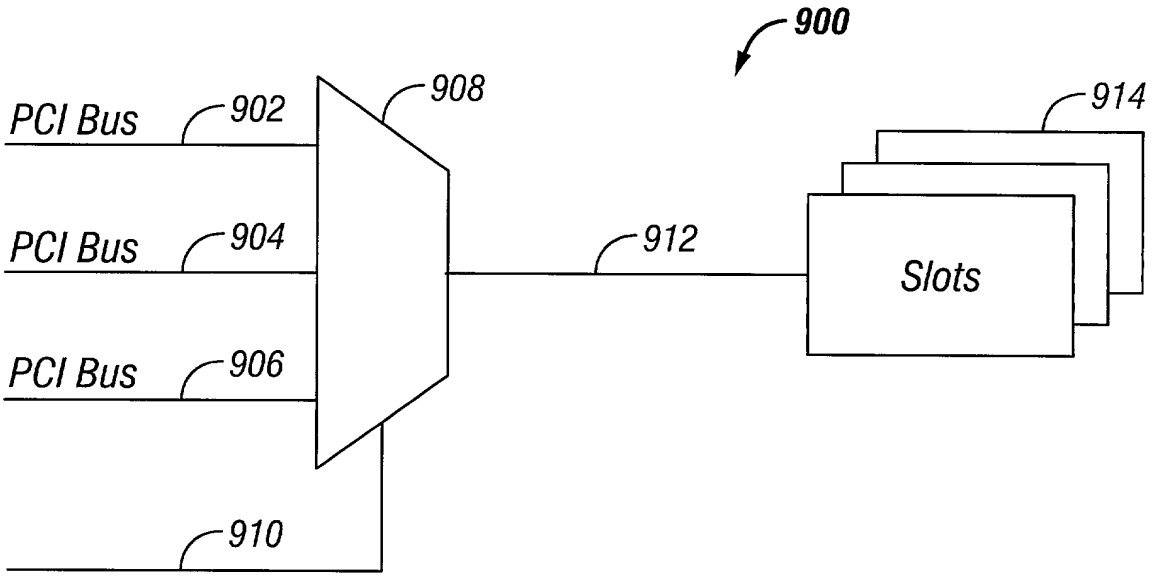
900
908
PCI Bus
902
914
PCI Bus
904
912
Slots
PCI Bus
906
910

FIG. 9